What is claimed is:

1. A semiconductor package comprising:

a semiconductor substrate;

a plurality of chip pads separately formed on an upper surface of the semiconductor substrate;

an irregular metal pattern electrically connected to the plurality of chip pads; and

an external terminal electrically connected to the metal pattern.

2. A semiconductor package comprising:

a semiconductor substrate;

a plurality of chip pads separately formed on an upper surface of the semiconductor substrate;

a first metal pattern formed on upper surfaces of the plurality of chip pads;

a second metal pattern having an irregular shape and formed on an upper surface of the first metal pattern; and

an external terminal electrically connected to the second metal pattern.

3. The semiconductor package according to claim 2, wherein the first metal pattern includes titanium.

4. The semiconductor package according to claim 2, wherein the second metal pattern includes nickel.

5. The semiconductor package according to claim 2, further comprising:

a first insulation layer formed on a region of the upper surface of the semiconductor substrate not occupied by the plurality of chip pads; and

a second insulation layer formed on upper surfaces of the first insulation layer and the first metal pattern.

6. The semiconductor package according to claim 5, wherein the first insulation layer includes polymide or benzocyclobutene.

7. The semiconductor package according to claim 5, wherein the second insulation layer includes a photoresist layer or benzocyclobutene.

8. The semiconductor package according to claim 5, further comprising a solder mask formed on an upper surface of the second insulation layer.

9. The semiconductor package according to claim 5, wherein the external terminal includes a solder ball.

10. The semiconductor package according to claim 9, wherein the semiconductor substrate includes a wafer.

11. A method of fabricating a semiconductor package comprising the steps of:

separately forming a plurality of chip pads on an upper surface of a semiconductor substrate;

forming an irregular metal pattern electrically connected to the plurality of chip pads; and

forming an external terminal electrically connected to the metal pattern.

12. A method of fabricating a semiconductor package comprising the steps of:

separately forming a plurality of chip pads on an upper surface of a semiconductor substrate;

forming a first metal pattern on upper surfaces of the plurality of chip pads;

forming a second metal pattern having an irregular shape on an upper surface of the first metal pattern; and

forming an external terminal electrically connected to the second metal pattern.

13. The method according to claim 12, further comprising the step of forming a first insulation layer on a region of the upper surface of the semiconductor substrate not occupied by the plurality of chip pads.

14. The method according to claim 13, wherein the step of forming the second metal pattern comprises:

coating a photoresist layer on the upper surface of the first metal pattern;

forming an irregular photoresist layer pattern and a second insulation layer by patterning the photoresist layer;

forming a metal layer in a space of the irregular photoresist layer pattern; and

removing the irregular photoresist layer pattern.

15. The method according to claim 14, wherein the step of forming the metal layer in the space of the irregular photoresist layer pattern is carried out according to an electro-plating process.

16. The method according to claim 14, further comprising a step of forming a solder mask on an upper surface of the second insulation layer so that a region of the second metal pattern is exposed.

17. The method according to claim 16, wherein the step of forming the external terminal comprises the steps of:

coating a solder paste on upper surfaces of the solder mask and the second metal pattern; and

performing a reflow process on the solder paste.

18. The method according to claim 13, wherein the step of forming the second metal pattern comprises the steps of:

coating a photoresist layer on the upper surface of the first metal pattern;

forming an irregular photoresist layer pattern by patterning the photoresist layer;

forming a metal layer in a space of the irregular photoresist layer pattern;

removing all the photoresist layers including the irregular photoresist pattern;

coating a second insulation layer on the upper surface of the first metal pattern; and

patterning the second insulation layer so that the upper and side portions of the metal layer are exposed.

19. The method according to claim 18, wherein the step of forming the external terminal comprises the steps of:

coating a solder paste on upper surfaces of the second insulation layer and the second metal pattern; and

performing a reflow process on the solder paste.

20. The method according to claim 12, wherein the first metal pattern includes titanium and the second metal pattern includes nickel.